

FORM PTO-1449/A and B (Modified) INFORMATION DISCLOSURE STATEMENT BY APPLICANT		APPLICATION NO.: 10/020,004	ATTY. DOCKET NO.: H0498.70164US00
		FILING DATE: December 11, 2001	CONFIRMATION NO.: 7232
		APPLICANT: Charles M. Lieber, et al.	
		GROUP ART UNIT: 2826	EXAMINER: Greene, Pershelle L.
Sheet	1	of	1

U.S. PATENT DOCUMENTS

Examiner's Initials	Cite No.	U.S. Patent Document		Name of Patentee or Applicant of Cited Document	Date of Publication or of issue of Cited Document MM-DD-YYYY
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FOREIGN PATENT DOCUMENTS

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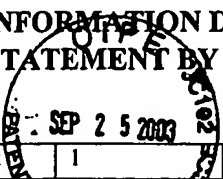
OTHER ART — NON PATENT LITERATURE DOCUMENTS

Examiner's Initials	Cite No	Include name of the author (in CAPITAL LETTERS) title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, relevant page(s), volume-issue number(s), publisher, city and/or country where published.	Translation (Y/N)	
W		Office Action mailed 09/02/2003 in co-pending U.S. Patent Application No. 09/935,776, filed 08/22/2001		
W		Haraguchi et al., Applied Physics Letters, V60, 1992, p.745-747		
W		Yu et al, Applied Physics Letters, V72, 1998, p. 3458-3460		
W		Esfarjani et al., Applied Physics Letters, V74, 1999, p. 79-81		
		Yamada, Applied Physics Letters, V76, 2000, p. 628-630		

EXAMINER 	DATE CONSIDERED 5/28/07
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#EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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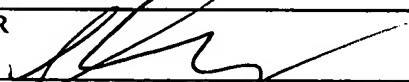
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<i>W</i>		US-2001/0054709		Heath et al.	

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<i>W</i>		CHUNG ET AL., <i>Applied Physics Letters</i> , V76, N15, 2000, pp. 2069-2070	
<i>W</i>		DUAN ET AL., "Nanoscale electronic and optoelectronic devices assembled from indium phosphide nanowire building blocks", supplementary article, <i>Nature</i> , 2001, vol. 409, pp. 66-69	
<i>W</i>		MORALES ET AL., <i>Science</i> , V279, 1998, pp. 208-211	
<i>W</i>		TANS ET AL., <i>Nature</i> , V393, 1998, pp. 49-52	
<i>W</i>		WOLF ET AL., "Silicon Processing for the VLSI Era", Lattice Press, V1, 2000, pp 12-13	

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